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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,813	SPRUNT ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-9,18,20,21 and 27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,18,20,21 and 27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 30, 2004 has been entered. Claims 1-4, 7-9, 18, 20, 21 and 27-45 are pending and have been examined.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4, 7-9, 18, 20, 21 and 25-29 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant contends that Larsen does not teach or reasonably suggest executing a plurality of threads simultaneously (page 9, first paragraph). However, as presented in the previous Office action, Larsen teaches a multithreaded processor. Specifically, Larsen discloses the "fine-grained multithreading supported by processor 10" (see processor 10 in FIG. 1, and column 3, lines 45-50). Larsen further discloses, "although processor 10 will hereafter be described as supporting only two concurrent threads (i.e., one active and one inactive), the present invention is equally applicable to multithreaded processors that support additional active and inactive threads" (see column 3, lines 50-55). Therefore, Larsen discloses executing at least two threads concurrently, or in other words, executing a plurality of threads simultaneously.

4. Applicant further contends that Larsen does not teach or reasonably suggest that the qualifying of the event is performed using a thread ID and a thread current privilege level (CPL),

the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (page 9, first paragraph).

However, such limitations were addressed in the previous Office action with regard to Larsen in view of Dreyer (for example, claims 25 and 26). The claim rejections presented below now reflect the new scope of the claims as amended.

Claim Objections

5. Claim 33 is objected to because of the following informalities: The claim recites, "The apparatus of claim 32 ..." in line 1. Base claim 32 recites a system, rather than an apparatus. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2-4, 7 and 8 are now rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 2 recites the limitation "wherein the access location ..." in line 1. There is insufficient antecedent basis for this limitation in the claim. Base claim 1, as amended, does not recite an access location. Claims 3 and 4 are dependent upon claim 2 and are thus indefinite for at least the same reason.

Claim 7 recites the limitation "wherein the event counter ..." in line 1. There is insufficient antecedent basis for this limitation in the claim. Base claim 1, as amended, does not recite an event counter. Claim 8 is dependent upon claim 7 and is thus indefinite for at least the same reason.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 7-9, 18, 20, 21, 27-34 and 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,835,705 to Larsen et al. (art of record; herein "Larsen") in view of U.S. Pat. No. 5,657,253 to Dreyer et al. (art of record; herein "Dreyer").

With respect to claim 1 (currently amended), Larsen discloses an apparatus comprising:

(a) a processor to execute a plurality of threads simultaneously, each thread including a series of instructions (see processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) an event detector to detect a predetermined list of events and to transmit an event detection signal to a multiplexer (see performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a

predetermined list of events; see also column 5, lines 7-17, which shows transmitting event signals to the multiplexer); and

(c) an event selection control register (ESCR) to instruct the multiplexer to select an event from the predetermined list of events by qualifying the event based on a set of conditions (see control registers 80 in FIG. 2, and column 5, lines 7-17, which shows the control registers selecting or qualifying events based on the mode of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which the events correspond, i.e. the source thread of the plurality of threads where the events occurred).

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID (see above), Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread current privilege level (CPL).

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see Dreyer, column 4, line 60 to column 5, line 3).

With respect to claim 2 (previously presented), Larsen further discloses the limitation wherein the access location allows access to determine the count without disturbing the operation

of event counter (see integer registers 38 in FIG. 1 and performance monitor counters 84 in FIG. 2, and column 7, lines 40-52, which shows accessing the registers to read a count without disturbing the operation of the counters).

With respect to claim 3 (previously presented), Larsen further discloses the limitation wherein the ESCR comprises a first field of bits to choose the event to be counted (see column 5, lines 7-17, which shows the control registers having bit fields to select the events to be counted).

With respect to claim 7 (previously presented), although Larsen discloses software-writable event counters (see column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is stopped and cleared before a new event is selected.

However, Dreyer discloses resetting, i.e. stopping and clearing, the event counter using an instruction (see column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter reset feature taught by Dreyer, for the purpose of stopping and clearing the counter values in software.

With respect to claim 8 (previously presented), although Larsen discloses software-writable event counters (see column 4, lines 50-57), Larsen does not expressly disclose the limitation wherein the event counter is preset to a certain state.

However, Dreyer discloses presetting the event counter to a certain value or state (see column 3, lines 19-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter preset feature taught by Dreyer, for the purpose of enabling functions such as countdowns (see Dreyer, column 4, lines 21-30).

With respect to claim 9 (previously presented), Larsen further discloses the limitation wherein the predetermined list of events includes hardware performance and breakpoint events (see column 5, lines 46-56, which shows the predetermined list of events, including hardware performance events such as instructions completed and processor cycles, along with breakpoint events such as thread switch counts).

With respect to claim 18 (currently amended), Larsen discloses a method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions (see processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) detecting a predetermined list of events and transmitting an event detection signal to a multiplexer (see performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events; see also column 5, lines 7-17, which shows transmitting event signals to the multiplexer);

(c) instructing the multiplexer to select and event from the predetermined list of events by qualifying the event based on a set of conditions (see control registers 80 in FIG. 2, and column 5, lines 7-17, which shows the control registers selecting or qualifying events based on the mode

of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which the events correspond, i.e. the source thread of the plurality of threads where the events occurred);

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID (see above), Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see Dreyer, column 4, line 60 to column 5, line 3).

Larsen further discloses:

(d) counting the event qualified by the multiplexer using an event counter (see performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) accessing the event counter to determine a current count of the event (see integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to

the integer registers, i.e. the access locations; see also column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 20 (previously presented), Larsen further discloses the limitation wherein the qualifying of the event includes requiring that the event has a preselected thread ID (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which they correspond).

With respect to claim 21 (currently amended), Larsen in view of Dreyer further discloses the limitation wherein the qualifying of the event further includes requiring that the event has a preselected thread CPL (see Dreyer, column 4, lines 39-46, which shows control register bits for enabling event counting based on the current privilege level).

With respect to claim 27 (currently amended), Larsen in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 28 (previously presented), Larsen further discloses the limitation wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which they correspond).

With respect to claim 29 (previously presented), Larsen in view of Dreyer further discloses the limitation wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred (see Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 30 (new), Larsen in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 31 (new), Larsen further discloses:

(a) an event counter to count the event qualified by the multiplexer (see performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(b) an access location to allow access to the event counter to determine a current count of the event (see integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations; see also column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 32 (new), Larsen discloses an apparatus comprising:

(a) a storage medium coupled with a processor (see main memory 52 and processor 10 in FIG. 1), the processor to execute a plurality of threads simultaneously, each thread including a

series of instructions (see column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) an event detector to detect a predetermined list of events and to transmit an event detection signal to a multiplexer (see performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events; see also column 5, lines 7-17, which shows transmitting event signals to the multiplexer); and

(c) an event selection control register (ESCR) to instruct the multiplexer to select an event from the predetermined list of events by qualifying the event based on a set of conditions (see control registers 80 in FIG. 2, and column 5, lines 7-17, which shows the control registers selecting or qualifying events based on the mode of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which the events correspond, i.e. the source thread of the plurality of threads where the events occurred).

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID (see above), Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see Dreyer, column 4, line 60 to column 5, line 3).

Larsen further discloses:

(d) an event counter to count the event qualified by the multiplexer (see performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) an access location to allow access to the event counter to determine a current count of the event (see integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations; see also column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 33 (new), the limitations recited in the claim are analogous to those of claim 2 (see the reasoning applied to claim 2 above).

With respect to claim 34 (new), the limitations recited in the claim are analogous to those of claim 3 (see the reasoning applied to claim 3 above).

With respect to claim 36 (new), the limitations recited in the claim are analogous to those of claim 2 (see the reasoning applied to claim 7 above).

With respect to claim 37 (new), the limitations recited in the claim are analogous to those of claim 2 (see the reasoning applied to claim 8 above).

With respect to claim 38 (new), the limitations recited in the claim are analogous to those of claim 2 (see the reasoning applied to claim 9 above).

With respect to claim 39 (new), the limitations recited in the claim are analogous to those of claim 2 (see the reasoning applied to claim 30 above).

With respect to claim 40 (new), Larsen discloses a machine-readable medium having stored thereon data representing sets of instructions (see column 3, lines 11-19, which shows a machine-readable medium having instructions stored thereon) the sets of instructions which, when executed by a machine (see column 4, lines 25-28, which shows executing the instructions), cause the machine to:

(a) execute a plurality of threads simultaneously, each thread including a series of instructions (see processor 10 in FIG. 1, and column 3, lines 39-55, which shows the multithreaded processor concurrently or simultaneously executing at least two threads, i.e. a plurality of threads, each comprising a group of instructions);

(b) detect a predetermined list of events and transmitting an event detection signal to a multiplexer (see performance monitor 50 and multiplexer 82 in FIG. 2, and column 4, lines 50-57, which shows the performance monitor, i.e. the event detector, detecting a predetermined list of events; see also column 5, lines 7-17, which shows transmitting event signals to the multiplexer);

(c) instruct the multiplexer to select and event from the predetermined list of events by qualifying the event based on a set of conditions (see control registers 80 in FIG. 2, and column 5, lines 7-17, which shows the control registers selecting or qualifying events based on the mode

of operation and other conditions), wherein the qualifying of the event is performed using a thread ID, the thread ID indicating a source of the event, the source including a thread of the plurality of threads where the event occurred (see column 6, line 54 to column 7, line 3, which shows selecting and routing events based on the identity of the thread or the thread ID to which the events correspond, i.e. the source thread of the plurality of threads where the events occurred);

Although Larsen discloses the limitation wherein the qualifying of the event is performed using a thread ID (see above), Larsen does not expressly disclose the limitation wherein the qualifying of the event is performed using a thread CPL.

However, Dreyer discloses control register bits for enabling event counting based on the current privilege level (see column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the CPL feature taught by Dreyer, for the purpose of differentiating and qualifying events based on supervisor and application levels of operation (see Dreyer, column 4, line 60 to column 5, line 3).

Larsen further discloses:

(d) count the event qualified by the multiplexer using an event counter (see performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows the counters recording or counting the events qualified by the multiplexer); and

(e) access the event counter to determine a current count of the event (see integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to

the integer registers, i.e. the access locations; see also column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 41 (new), the limitations recited in the claim are analogous to those of claim 20 (see the reasoning applied to claim 20 above).

With respect to claim 42 (new), the limitations recited in the claim are analogous to those of claim 21 (see the reasoning applied to claim 21 above).

With respect to claim 43 (new), the limitations recited in the claim are analogous to those of claim 27 (see the reasoning applied to claim 27 above).

With respect to claim 44 (new), the limitations recited in the claim are analogous to those of claim 28 (see the reasoning applied to claim 28 above).

With respect to claim 45 (new), the limitations recited in the claim are analogous to those of claim 29 (see the reasoning applied to claim 29 above).

10. Claims 4 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen in view of Dreyer, as applied to claims 3 and 34 above, respectively, and further in view of U.S. Pat. No. 6,205,468 to Diepstraten et al. (art of record; herein "Diepstraten").

With respect to claim 4 (previously presented), although Larsen discloses control registers with bit fields for selecting events to be recorded, setting the mode of operation, and enabling or disabling event counting (see column 5, lines 7-17), Larsen does not expressly

disclose the limitation wherein the ESCR further comprises a second field of bits to choose the event to be masked and not counted.

However, Diepstraten discloses an event masker associated with an event recorder having control bits for masking events (see event mask register 90 in FIG. 3, and column 4, lines 42-50, which shows masking events to select one or more events to be ignored, i.e. not counted).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the event masking feature taught by Diepstraten, for the purpose of reducing the number of events that will be processed (see Diepstraten, column 4, lines 42-50).

With respect to claim 35 (new), the limitations recited in the claim are analogous to those of claim 4 (see the reasoning applied to claim 4 above).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

After October 25, 2004, the examiner can be reached at (571) 272-3707, and the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3694.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy

ANTONY NGUYEN-BA
PRIMARY EXAMINER